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EXAMINER	
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ART UNIT	PAPER NUMBER
2813	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/685,055	KUMAR ET AL.	
	Examiner	Art Unit	
	Heather A. Doty	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-24 and 50-72* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *69-72* is/are allowed.

6)☒ Claim(s) *1,3-13,18-24 and 50-68* is/are rejected.

7)☒ Claim(s) *14-17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 52 is objected to because of the following informalities: In line 2 of claim 52, "to form" should be deleted. Appropriate correction is required.

Claim 57 is objected to because of the following informalities: Claim 57 should be changed to depend from claim 56, and not from itself. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless – (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 4-6, 9, 10, and 22-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Kihara et al. (JP 2002-124568, published 26 April 2002), using U.S. 2004/0026364 as a translation.

Regarding claim 1, Kihara et al. teaches a method of fabricating a semiconductor device, the method comprising:

- providing a workpiece (Fig 4A);
- disposing a first dielectric material over the workpiece (FSG layer **204** in Fig. 4A);
- disposing a second dielectric material (SiLK layer **206**) in Fig. 4A) defining a top surface (paragraph 0049—layer 206 is the top layer before the hardmask is formed) comprising a different material with different etching

characteristics (paragraph 0015; Fig. 6) than the first dielectric material, wherein the first dielectric material and the second dielectric material comprise a first insulating layer;

- forming a first pattern in the first dielectric material by a first etching process, said first etching process selective to said second dielectric material (Fig. 5B; paragraph 0055—Fig. 6 shows that this etch selectively etches FSG over SiLK); and forming a second pattern in the second dielectric material (Fig. 5C) by a second etching process, said second etching process selective to said first dielectric material (the SilK etch used in this reference, N_2 and H_2—see paragraph 0053—does not etch FSG, as shown in Fig. 6), the second pattern being different from the first pattern (Fig. 5C); and
- depositing a conductive material over the patterned second dielectric material and the patterned first dielectric material (paragraph 0057), wherein said first dielectric material has a coefficient of thermal expansion (CTE) substantially similar to the CTE of the conductive material (this is inherently so, as the instant specification teaches that FSG is a material with a CTE compatible with copper—see paragraphs 0031-0032).

Regarding claim 4, Kihara et al. teaches the method of claim 1, and further teaches that the conductive material forms vias in the first pattern of the first dielectric material (paragraph 0057).

Regarding claim 5, Kihara et al. teaches the method of claim 4, and further teaches that the vias comprise substantially vertical sidewalls (Fig. 5D).

Regarding claim 6, Kihara et al. teaches the method of claim 4, and further teaches that the workpiece comprises component regions, wherein at least one of the vias makes electrical contact with a component region of the workpiece (paragraph 0002 discloses that the purpose of the via is to connect elements arranged along the vertical direction in a multilayer semiconductor structure).

Regarding claim 9, Kihara et al. teaches the method of claim 1, and further teaches depositing a hard mask over the second dielectric material (SiON layer **208** in Fig. 2A or **308** in Fig. 4A).

Regarding claim 10, Kihara et al. teaches the method of claim 9, and further teaches depositing a first mask layer (**208** in Fig. 2A); depositing a second mask layer over the first mask layer (**210** in Fig. 2A); and depositing a third mask layer over the second mask layer (**214/216** in Fig. 2C; paragraph 0039).

Regarding claims 22 and 24, Kihara et al. teaches the method of claim 1, and further teaches that disposing the first dielectric material comprises disposing an inorganic material (paragraphs 0015 and 0037, FSG—further limited by claim 24), and wherein disposing the second dielectric material comprises disposing an organic material (paragraphs 0015 and 0037, SilK—further limited by claim 24).

Regarding claim 23, Kihara et al. teaches the method according to claim 1, and further teaches that disposing the first dielectric material comprises disposing a material that is etchable selective to the second dielectric material (paragraph 0015; Fig. 6).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 7, 8, 13, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kihara et al. (JP 2002-124568, published 26 April 2002), using U.S. 2004/0026364 as a translation, in view of Bekiaris et al. (U.S. 2003/0119307).

Regarding claim 3, Kihara et al. teaches the method of claim 1 (note 35 U.S.C. 102(b) rejection above), but does not expressly teach removing the conductive material from the top surface of the second dielectric material to form conductive lines in the second pattern of the second dielectric material.

Bekiaris et al. teaches a method of depositing a conductive material over a patterned second dielectric material and patterned first dielectric material, further comprising removing the conductive material from the top surface of the second dielectric material to form conductive lines in the second pattern of the second dielectric material (Fig. 3, paragraph 0033).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of Kihara et al. and Bekiaris and use the method taught by Kihara et al. and further remove the conductive material from the top surface of the second dielectric material to form conductive lines in the second pattern of the second dielectric material, as taught by Bekiaris et al., since Bekiaris et al.

teaches that this is an effective method to complete a dual damascene structure (paragraph 0033).

Regarding claims 7 and 8, Kihara et al. teaches the method of claim 6 (note 35 U.S.C. 102(b) rejection above), but does not teach that the workpiece component regions comprise a plurality of conductive lines formed in a dielectric layer, or that the lines comprise copper.

Bekiaris et al. teaches that a substrate suitable for a dual-damascene process may include a plurality of copper conductive lines formed in a dielectric layer (paragraph 0035).

Therefore, at the time of the invention, it would have been obvious to use the dual-damascene method taught by Kihara et al. and the substrate containing copper conductive lines formed in a dielectric material, since Bekiaris et al. teaches that such a substrate is appropriate for use with a dual-damascene method.

Regarding claim 13, Kihara et al. teaches the method of claim 10 (note 35 U.S.C. 102(b) rejection above, and further teaches patterning the third mask layer, the second mask layer, and the first mask layer with the first pattern (Fig. 2F), transferring the first pattern to the second dielectric material (Fig. 3A), removing the third mask layer, the second mask layer, and the first mask layer in the second pattern regions (Fig. 3B), transferring the first pattern to the first dielectric material (Fig. 3B), and removing the second dielectric material in the second pattern regions (Fig. 3C). Kihara et al. does not teach patterning at least the third mask layer with the second pattern.

Bekiaris et al. teaches a dual-damascene process comprising patterning at least a third mask layer with the second pattern (Fig. 5F).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Kihara et al., and pattern the third mask layer with the second pattern, as taught by Bekiaris et al. The motivation for doing so at the time of the invention would have been that if the third mask layer is deposited before the second mask layer is patterned with the second pattern, so that the third mask layer is also patterned with the second pattern, the third mask layer will protect the second mask layer during the removal of the photoresist layer used to pattern the hard mask layers, as taught by Bekiaris et al. (paragraph 0040).

Regarding claim 18, Kihara et al. and Bekiaris et al. together teach the method according to claim 13. Bekiaris et al. further teaches depositing a cap layer (**112** in Fig. 5L) over the workpiece, before disposing the first dielectric material, and transferring the first pattern to the cap layer (Fig. 5L).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Kihara et al. and Bekiaris et al. together, and further deposit a cap layer over the workpiece before disposing the first dielectric material, and transfer the first pattern to the cap layer, as further taught by Bekiaris. The motivation for doing so at the time of the invention would have been that the cap layer is a barrier dielectric layer (Bekiaris et al., paragraph 0036), and in order to contact the underlying electrical elements with the via metallization, the cap layer must also acquire the first pattern (Fig. 5L).

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kihara et al. (JP 2002-124568, published 26 April 2002), using U.S. 2004/0026364 as a translation, in view of Bekiaris et al. (U.S. 2003/0119307) and Wolf et al. (*Silicon Processing for the VLSI Era*, vol. 1, 2nd edition, 2000).

Regarding claim 21, Kihara et al. and Bekiaris et al. together teach the method according to claim 13 (note 35 U.S.C. 103(a) rejection above). Bekiaris et al. further teaches that forming the first pattern and the second pattern further comprises:

after patterning at least the third mask layer with the second pattern, depositing an anti-reflective coating over the first mask layer (**140** in Fig. 5H; paragraph 0044);

depositing a photoresist layer over the anti-reflective coating (**142** in Fig. 5H; paragraph 0044);

patterning the photoresist with the first pattern (**134** in Fig. 5H; paragraph 0045);

and transferring the first pattern in the photoresist layer to the third mask layer, the second mask layer, the first mask layer, and the second dielectric layer (Fig. 5I; paragraph 0046).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Kihara et al. and Bekiaris et al. together, and further deposit an antireflective coating over the first mask layer after patterning the third mask layer with the second pattern, deposit a photoresist layer over the antireflective coating, pattern the photoresist with the first patter, and transfer the first pattern to the third mask layer, the second mask layer, the first mask layer, and the second dielectric layer, as taught by Bekiaris et al. The motivation for doing so at the

time of the invention would have been to provide linewidth control during photolithography by reducing reflectivity at the resist interface, as taught by Wolf et al. (p. 524, section 12.4.2.6).

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kihara et al. (JP 2002-124568, published 26 April 2002), using U.S. 2004/0026364 as a translation, in view of Hsue et al. (U.S. 2003/0044725).

Regarding claim 11, Kihara et al. teaches the method according to claim 10 (note 35 U.S.C.102(b) rejection above), but does not teach that depositing the first mask layer comprises depositing SiC_x, SiC_xN_x, SiC_xH_y, $SiC_xN_yH_z$, or SiCOH, wherein depositing the second mask layer comprises depositing Si_xN_y or SiO_2, and wherein depositing the third mask layer comprises depositing a refractory metal nitride.

Hsue et al. teaches a dual-damascene method with a low-k dielectric layer and multilayer hard mask, the hard mask layers comprising SiC, SiN, SiO_2, or a refractory metal nitride, TaN (paragraph 0026).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Kihara et al., and further form the first hard mask layer of SiC, the second hard mask layer of SiN or SiO_2, and the third hard mask layer of TaN, since Hsue et al. teaches that these materials are appropriate to use as hard mask layers in dual-damascene applications involving low-k dielectrics (paragraph 0026).

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kihara et al. (JP 2002-124568, published 26 April 2002), using U.S. 2004/0026364 as a

translation, in view of Hsue et al. (U.S. 2003/0044725) as applied to claim 11 above, and further in view of Soda (U.S. 2003/0054656).

Regarding claim 12, Kihara et al. and Hsue et al. together teach the method according to claim 11 (note 35 U.S.C. 103(a) rejection above), but they do not teach a hard mask layer comprising the combination of a layer of SiC_x and a layer of N-SiC_x over the layer of SiC_x.

Soda et al. teaches a dual-damascene method employing a hard mask layer comprised of a layer of SiC_x and a layer of SiCN (paragraph 0121).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Kihara et al. and Hsue et al. together, and further fabricate the first mask layer of a layer of SiC_x and a layer of SiCN, as taught by Soda to be known in the art as appropriate for dual-damascene applications.

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kihara et al. (JP 2002-124568, published 26 April 2002), using U.S. 2004/0026364 as a translation, in view of Bekiaris et al. (U.S. 2003/0119307), as applied to claim 18 above, and further in view of Tsai et al. (U.S. 2002/0164889).

Regarding claim 19, Kihara et al. and Bekiaris et al. together teach the method according to claim 18 and 1 (note 35 U.S.C. 103(a) rejection above), but do not teach forming an adhesion film over a top surface of the cap layer.

Tsai et al. teaches forming a cap layer over a semiconductor structure, depositing an adhesion layer over the cap layer, and forming a low-k dielectric over the

adhesion layer, to improve the adhesion of the low-k layer to the adjacent layer (paragraph 0012).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Kihara et al, Bekiaris et al. together, and further form an adhesion film over a top surface of the cap layer in order to improve the adhesion of the dielectric layer to the adjacent layers, as taught by Tsai et al.

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kihara et al. (JP 2002-124568, published 26 April 2002), using U.S. 2004/0026364 as a translation, in view of Tsai et al. (U.S. 2002/0164889).

Regarding claim 20, Kihara et al. teaches the method of claim 1 (note 35 U.S.C. 102(b) rejection above), but does not teach forming an adhesion film disposed over a top surface of the first dielectric layer.

Tsai et al. teaches forming a cap layer over a semiconductor structure, depositing an adhesion layer over the cap layer, and forming a low-k dielectric over the adhesion layer, and additionally over the first dielectric layer, to improve the adhesion of the low-k layer to the adjacent layer (paragraph 0012).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of Kihara et al. and Tsai et al. by using the method taught by Kihara et al., and further form an adhesion film over a top surface of the cap layer and over the top surface of the first dielectric layer in order to improve the adhesion of the dielectric layer to the adjacent layers, as taught by Tsai et al.

Claims 50-57, 62, and 66-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kihara et al. (JP 2002-124568, published 26 April 2002), using U.S. 2004/0026364 as a translation in view of Ou-Yang et al. (U.S. 2002/0074312) and Bekiaris et al. (U.S. 2003/0119307).

Regarding claim 50, Kihara et al. teaches a method of fabricating a semiconductor device, the method comprising:

- disposing a workpiece (**W** in Fig. 1) in a processing chamber (**104** in Fig. 1);
- disposing a first dielectric material over the workpiece (FSG layer 204 in Fig. 4A);
- disposing a second dielectric material (SiLK layer 206) in Fig. 4A) over the first dielectric material, the second dielectric material comprising a different material (paragraph 0015; Fig. 6) than the first dielectric material, wherein the first dielectric material and the second dielectric material comprise a first insulating layer;
- depositing a hard mask over the second dielectric material, the depositing of said hard mask comprising depositing a first mask layer, depositing a second mask layer over said first mask layer and depositing a third mask layer over the second mask layer (layers **208**, **210**, and **214/216** respectively);
- forming a first pattern in the first dielectric material (Fig 2E);

- forming a second pattern different from the first pattern in the second dielectric material (Fig. 3C), wherein forming said pattern comprises:
- patterning the third mask layer, the second mask layer, and the third mask layer with the first pattern (Fig. Fig. 2E);
- transferring the first pattern to the second dielectric material (Fig. 2E);
- removing the third mask layer, the second mask layer, and the first mask layer in the second pattern regions (Fig. 3B);
- transferring the first pattern to the first dielectric material (Fig. 3B); and
- removing the second dielectric material in the second pattern regions (Fig. 3C).

Kihara et al. does not teach cleaning the processing chamber while the workpiece remains in the processing chamber or patterning at least the third mask layer with the second pattern.

Ou-Yang et al. teaches a method of cleaning a process chamber after a dielectric etch while the workpiece remains in the processing chamber (paragraph 0017). Ou-Yang teaches that this cleaning step provides a stabilized chamber condition for future processing steps.

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Kihara et al., and further clean the process chamber while the workpiece remains in the chamber to provide a stabilized chamber condition for future processing steps. Note that as currently written, claim 1

does not require this cleaning step to be performed at any particular point or time in the method.

Bekiaris et al. teaches a dual-damascene process comprising patterning at least a third mask layer with the second pattern (Fig. 5F).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Kihara et al. and Ou-Yang et al., and pattern the third mask layer with the second pattern, as taught by Bekiaris et al. The motivation for doing so at the time of the invention would have been that if the third mask layer is deposited before the second mask layer is patterned with the second pattern, so that the third mask layer is also patterned with the second pattern, the third mask layer will protect the second mask layer during the removal of the photoresist layer used to pattern the hard mask layers, as taught by Bekiaris et al. (paragraph 0040).

Regarding claims 51-53, Kihara et al., Ou-Yang et al., and Bekiaris et al. together teach the method of claim 50. Kihara et al. further teaches that the second dielectric material comprises a top surface (paragraph 0049—layer 206 is the top layer before the hardmask is formed), and further teaches depositing a conductive material over the patterned second dielectric material and the patterned first dielectric material (paragraph 0057), but does not expressly teach removing the conductive material from the top surface of the second dielectric material.

Bekiaris et al. teaches a method of depositing a conductive material over a patterned second dielectric material and patterned first dielectric material, further

comprising removing the conductive material from the top surface of the second dielectric material to form conductive lines in the second pattern of the second dielectric material and vias in the first pattern of the first dielectric material (Fig. 3, paragraph 0033).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Kihara et al., Ou-Yang et al., and Bekiaris et al., and further remove the conductive material from the top surface of the second dielectric material to form conductive lines in the second pattern of the second dielectric material and vias in the first pattern of the first dielectric material, as taught by Bekiaris et al., since Bekiaris et al. teaches that this is an effective method to complete a dual damascene structure (paragraph 0033).

Regarding claim 54, Kihara et al. Ou-Yang et al., and Bekiaris et al. together teach the method of claim 53. Kihara et al. further teaches that the vias comprise substantially vertical sidewalls (Fig. 5D).

Regarding claim 55, Kihara et al. Ou-Yang et al., and Bekiaris et al. together teach the method of claim 53. Kihara et al. further teaches that the workpiece comprises component regions, wherein at least one of the vias makes electrical contact with a component region of the workpiece (paragraph 0002 discloses that the purpose of the via is to connect elements arranged along the vertical direction in a multilayer semiconductor structure).

Regarding claim 56, Kihara et al. Ou-Yang et al., and Bekiaris et al. together teach the method of claim 54. Bekiaris et al. further teaches that a substrate suitable for

a dual-damascene process may include a plurality of conductive lines formed in a dielectric layer (paragraph 0035).

Therefore, at the time of the invention, it would have been obvious to use the dual-damascene method taught by Kihara et al. and the substrate containing conductive lines formed in a dielectric material, since Bekiaris et al. teaches that such a substrate is appropriate for use with a dual-damascene method.

Regarding claim 57, Kihara et al. Ou-Yang et al., and Bekiaris et al. together teach the method of claim 56. Bekiaris et al. further teaches that the conductive lines comprise copper (paragraph 0035). Kihara et al. further teaches that disposing the first dielectric material comprises disposing a material having a CTE close to the CTE of the conductive lines (this is inherently so, as the instant specification teaches that FSG, the material Kihara et al. teaches for the first dielectric material, is a material with a CTE compatible with copper—see paragraphs 0031-0032).

Regarding claim 62, Kihara et al. Ou-Yang et al., and Bekiaris et al. together teach the method of claim 50. Bekiaris et al. further teaches depositing a cap layer (**112** in Fig. 5L) over the workpiece, before disposing the first dielectric material, and transferring the first pattern to the cap layer (Fig. 5L).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Kihara et al., Ou-Yang, and Bekiaris et al. together, and further deposit a cap layer over the workpiece before disposing the first dielectric material, and transfer the first pattern to the cap layer, as further taught by Bekiaris. The motivation for doing so at the time of the invention would have been that

the cap layer is a barrier dielectric layer (Bekiaris et al., paragraph 0036), and in order to contact the underlying electrical elements with the via metallization, the cap layer must also acquire the first pattern (Fig. 5L).

Regarding claims 66-68, Kihara et al. Ou-Yang et al., and Bekiaris et al. together teach the method of claim 50. Kihara et al. further teaches that disposing the first dielectric material comprises disposing an inorganic material, and wherein disposing the second dielectric material comprises disposing an organic material, that disposing the first dielectric material comprises disposing a material that is etchable selective to the second dielectric material (paragraph 0015; Fig. 6), and that disposing the first dielectric material comprises disposing FSG and that disposing the second dielectric material comprises disposing SiLK (paragraph 0037).

Claim 65 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kihara et al. (JP 2002-124568, published 26 April 2002), using U.S. 2004/0026364 as a translation, in view of Ou-Yang et al. (U.S. 2002/0074312), Bekiaris et al. (U.S. 2003/0119307), and Wolf et al. (Silicon Processing for the VLSI Era, vol. 2, 2nd edition, 2000).

Regarding claim 65, Kihara et al., Ou-Yang et al., and Bekiaris et al. together teach the method of claim 50. Bekiaris et al. further teaches that forming the first pattern and the second pattern further comprises:

after patterning at least the third mask layer with the second pattern, depositing an anti-reflective coating over the first mask layer (**140** in Fig. 5H; paragraph 0044);

depositing a photoresist layer over the anti-reflective coating (**142** in Fig. 5H; paragraph 0044);

patterning the photoresist with the first pattern (**134** in Fig. 5H; paragraph 0045);

and transferring the first pattern in the photoresist layer to the third mask layer, the second mask layer, the first mask layer, and the second dielectric layer (Fig. 5I; paragraph 0046).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Kihara et al., Ou-Yang et al., and Bekiaris et al. together, and further deposit an antireflective coating over the first mask layer after patterning the third mask layer with the second pattern, deposit a photoresist layer over the antireflective coating, pattern the photoresist with the first patter, and transfer the first pattern to the third mask layer, the second mask layer, the first mask layer, and the second dielectric layer, as taught by Bekiaris et al. The motivation for doing so at the time of the invention would have been to provide linewidth control during photolithography by reducing reflectivity at the resist interface, as taught by Wolf et al. (p. 524, section 12.4.2.6).

Claim 58 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kihara et al. (JP 2002-124568, published 26 April 2002), using U.S. 2004/0026364 as a translation, in view of Ou-Yang et al. (U.S. 2002/0074312) and Bekiaris et al. (U.S. 2003/0119307), as applied to claim 50 above, and further in view of Hsue et al. (U.S. 2003/0044725).

Regarding claim 58, Kihara et al. Ou-Yang et al., and Bekiaris et al. together teach the method of claim 50. They not teach that depositing the first mask layer comprises depositing SiC_x, SiC_xN_x, SiC_xH_y, $SiC_xN_yH_z$, or SiCOH, wherein depositing the second mask layer comprises depositing Si_xN_y or SiO_2, and wherein depositing the third mask layer comprises depositing a refractory metal nitride.

Hsue et al. teaches a dual-damascene method with a low-k dielectric layer and multilayer hard mask, the hard mask layers comprising SiC, SiN, SiO_2, or a refractory metal nitride, TaN (paragraph 0026).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Kihara et al., Ou-Yang et al., and Bekiaris et al. and further form the first hard mask layer of SiC, the second hard mask layer of SiN or SiO_2, and the third hard mask layer of TaN, since Hsue et al. teaches that these materials are appropriate to use as hard mask layers in dual-damascene applications involving low-k dielectrics (paragraph 0026).

Claim 59 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kihara et al. (JP 2002-124568, published 26 April 2002), using U.S. 2004/0026364 as a translation, in view of Hsue et al. (U.S. 2003/0044725), Ou-Yang et al. (U.S. 2002/0074312) and Bekiaris et al. (U.S. 2003/0119307), and Hsue et al. (U.S. 2003/0044725), as applied to claim 58 above, and further in view of Soda (U.S. 2003/0054656).

Kihara et al., Ou-Yang et al., Bekiaris et al., and Hsue et al. together teach the method of claim 58, but they do not teach a hard mask layer comprising the combination of a layer of SiC_x and a layer of N-SiC_x over the layer of SiC_x.

Soda et al. teaches a dual-damascene method employing a hard mask layer comprised of a layer of SiC_x and a layer of SiCN (paragraph 0121).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Kihara et al., Ou-Yang et al., Bekiaris et al, and Hsue et al. together, and further fabricate the first mask layer of a layer of SiC_x and a layer of SiCN, as taught by Soda to be known in the art as appropriate for dual-damascene applications.

Claims 60 and 61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kihara et al. (JP 2002-124568, published 26 April 2002), using U.S. 2004/0026364 as a translation, Ou-Yang et al. (U.S. 2002/0074312) and Bekiaris et al. (U.S. 2003/0119307), as applied to claim 50 above, and further in view of Poag et al. (U.S. 6,197,123).

Regarding claim 60, Kihara et al., Ou-Yang et al., and Bekiaris et al. together teach the method of claim 50, but do not teach that cleaning the processing chamber comprises introducing a plasma cleaning gas comprising O2 gas diluted in Ar, He, or N_2, or that the plasma cleaning gas removes polymer buildup on the processing chamber walls.

Poag teaches a method of removing polymer buildup on the processing chamber walls by introducing a plasma cleaning gas comprising O_2 gas diluted in Ar or N_2 (column 2, lines 19-26).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Kihara et al., Ou-Yang et al., and Bekiaris et al. together, and further remove polymer buildup on the processing chamber walls by introducing a plasma cleaning gas comprising O_2 gas diluted in Ar or N_2, as taught by Poag et al., since Poag et al. teaches that this is a method known in the art of semiconductor processing to effectively clean processing chambers.

Regarding claim 61, Kihara et al., Ou-Yang et al., Bekiaris et al., and Poag et al. together teach the method of claim 60. Ou-Yang et al. further teaches that the workpiece is not biased during the cleaning method (paragraph 0052). They do not specifically teach applying a plasma electrode power density of about 0.1 W/cm^2 to 10 W/cm^2 at a pressure of about 50 mTorr to 500 mTorr.

However, it has been held that where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller* 105 USPQ233, 255 (CCPA 1955).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Kihara et al., Ou-Yang et al., Bekiaris et al., and Poag et al. together, and further optimize the processing conditions to arrive at the claimed power density and pressure.

Claims 63 and 64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kihara et al. (JP 2002-124568, published 26 April 2002), using U.S. 2004/0026364 as a translation, in view of Ou-Yang et al. (U.S. 2002/0074312) and Bekiaris et al. (U.S. 2003/0119307), as applied to claims 50 and 62 above, and further in view of Tsai et al. (U.S. 2002/0164889).

Regarding claims 63 and 64, Kihara et al., Ou-Yang et al., and Bekiaris et al. together teach the method of claims 62 and 50, but do not teach forming an adhesion film over a top surface of the cap layer or disposed over a top surface of the first dielectric layer.

Tsai et al. teaches forming a cap layer over a semiconductor structure, depositing an adhesion layer over the cap layer, and forming a low-k dielectric over the adhesion layer, and additionally over the first dielectric layer, to improve the adhesion of the low-k layer to the adjacent layer (paragraph 0012).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Kihara et al., Ou-Yang et al., and Bekiaris et al. together, and further form an adhesion film over a top surface of the cap layer and over the top surface of the first dielectric layer in order to improve the adhesion of the dielectric layer to the adjacent layers, as taught by Tsai et al.

Allowable Subject Matter

For the reasons given in the Office action dated 10/3/2005, claims 14-17 are objected to as being dependent upon a rejected base claim, but would be allowable if

rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 69-72 are allowed. The following is a statement of reasons for the indication of allowable subject matter:

Prior art does not teach or suggest, in combination with the other claimed limitations, a method of fabricating a semiconductor device comprising the step of moving the workpiece to another processing chamber specifically before the step of removing the second dielectric material to form a second pattern.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather A. Doty, whose telephone number is 571-272-8429. The examiner can normally be reached on M-F, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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